A VLSI-BASED MULTI-LEVEL ECG COMPRESSION SCHEME FOR WEARABLE SENSOR NODE

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Abstract: Wearable sensor nodes, possessing constant monitoring features, produce a large amount of data. Besides, power consumption is a major constraint in these nodes in ensuring longer battery life as approximately 3/4th of the power of the sensor node is consumed during data transmission. During smart long-term monitoring of any biomedical signal in wireless body area networks, wearable sensor nodes generate and transmit a large amount of data, increasing transmission power consumption. In order to reduce data storage and power consumption, a lossless data compression technique for an electrocardiogram signal monitoring system is proposed. For this, a hybrid lossless multi-level compression algorithm based on Golomb–Rice coding and dictionary selection based on bitmask method is proposed to enhance the bit compressing rate. Golomb–Rice coding is one of the efficient lossless coding techniques that has been used where amplitude values of the input bit stream are significantly lower and with continuous runs of ones and zeros. An efficient bitmask with dictionary selection technique can create a large set of matching patterns that can significantly reduce the memory requirement for a set of repeated random data. The lossless encoding scheme is implemented on the MIT-BIH arrhythmia database, achieving a compression ratio better than the existing architecture.

Key words: High compression ratio, Wearable Sensor Nodes, Golomb–Rice coding, Compression Techniques

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Introduction:

Wearable sensor nodes, possessing constant monitoring features, produce a large amount of data. Besides, power consumption is a major constraint in these nodes in ensuring longer battery life as approximately 72% of the power of the sensor node is consumed during data transmission. Currently, sensor nodes in IoT-based wireless body area network systems acquire ECG signals and transmit the digitized version of the signal to a remotely located base station where off-node processing is carried out. Minimizing the transceiver usage through data compression in the sensor node is an efficient way to reduce power consumption. High compression ratio (CR) can be achieved through lossy compression techniques with the cost of reconstruction error. Several lossy compression schemes are implemented in and, where computationally complex algorithms extract features from a specific domain of the signal to achieve high CR.

Most of the lossy techniques require an efficient preprocessing stage for detecting the clinically important features with minimal reconstruction error. This in turn increases computational load. Also, transformation from one domain to another leads to the requirement of large storage space with increased latency. In the case of lossless compression, prediction-based techniques with Golomb–Rice encoding are employed. An adaptive linear predictor is implemented, and predicted difference is encoded with variable-length encoding. A VLSI-based adaptive linear predictor is discussed, where adaptive Golomb–Rice coding is used for entropy coding. A power-gating approach is utilized in compressed sensing for developing a low-power FPGA-based compression architecture. However, from the perspective of wearable node, these methods employ computationally intensive operations, affecting its area overhead and power consumption. For biomedical signal monitoring through wearable node, the VLSI-based lossless compression schemes with optimal area overhead and power consumption are highly demanded for real-time, online implementation on the wearable sensor node. However, it needs further study to find a better approach for improvement in CR, and as with the increase in transmitted data load in sensor node, the lifetime of the battery degrades significantly.

LITERATURE SURVEY

1) VLSI implementation of lossless ECG Compression Algorithm for Low Power Devices

In this paper VLSI implementation of lossless ECG Compression Algorithm for electrocardiogram (ECG) data encoding to save storage space and reduce transmission time is proposed. As compression algorithm is able to save storage space and reduce transmission time, this opportunity has been seized by implementing memory-less design. This brief presents a VLSI implementation of an efficient lossless compression scheme while working at a high clock speed in VLSI. ECG compression algorithm comprises two parts: an adaptive linear prediction technique

and content-adaptive Golomb Rice code. An efficient and low power VLSI implementation of compression algorithm has been presented. To improve the performance, the proposed VLSI design uses bit shifting operations as a replacement for the different arithmetic operations. VLSI implementation has been applied to the MIT-BIH arrhythmia database which is able to achieve a lossless bit compression rate of 2.77. Moreover, VLSI architecture contains 3.1 K gate count and core of the chip consumes 27.2 nW of power while working at 1 KHz frequency. The core area is 0.05 mm^2 in 90 nm CMOS process.

2) VLSI Implementation of Multi-Channel ECG Lossless Compression System

Electrocardiogram (ECG) is used to record the electrical activity of heart. If the instrument monitoring the signal for a long time, it will produce large amount of data. So, the effective lossless ECG compression system can help to reduce the storage space. This brief presents a hardware architecture of multi-channel lossless ECG compression system. The system is based on the algorithm including multi-channel linear prediction and adaptive linear prediction. Also, Golomb rice code (GRC) is used for entropy coding. The hardware implementation has been designed with low hardware complexity usage while using optimum hardware resources. And the architecture can process multiple channels in parallel that can obtain the high throughput. PTB database has been used for verification and testing purposes. This design was implemented in TSMC 180nm. The implementation results show the gate count is 476K and power consumption is 69.18µW while working frequency is 1 KHz.

3) A 2.63 µW ECG Processor with Adaptive Arrhythmia Detection and Data Compression for Implantable Cardiac Monitoring Device

An ultra-low power ECG processor ASIC (application specific integrated circuit) with R-wave detection and data compression is presented, which is designed for the long-term implantable cardiac monitoring (ICM) device for arrhythmia diagnosis. An adaptive derivative-based detection algorithm with low computation overhead for potential arrhythmia recording is proposed to detect arrhythmia with the occasional abnormal heart beats. In order to save as much as possible cardiac information with the limited memory size available in the ICM device, a hierarchical data buffer structure is proposed which saves 3 types of data, including the raw ECG

data segments of 2 seconds, compressed ECG data segments of 45 seconds, and R-peak values and interval lengths of >2000 beat cycles. A modified swinging-door-trending (SDT) method is proposed for the ECG data compression. The ASIC has been implemented based on fully-customized near-threshold standard cells using the thick-gate transistors in 65-nm CMOS technology for low dynamic power consumption and leakage. The ASIC core occupies a die area of 1.77 mm^2. The measured total power is 2.63 µW, which is among the ECG processors with the lowest core power consumption. It exhibits a relatively high positive precision rate (P_+) of 99.3% with a sensitivity of 98.2%, in contrast to the similar designs in literature with the same core power consumption level. Also, an ECG data compression ratio (CR) of up to 17.0 has been achieved, with a good trade-off between the compression efficiency and loss.

4) Lossless and Lossy Direct Compression Design with Multi-Signal Symptom Detection for Low-Temperature Wearable Devices

In this paper, the lossless and lossy direct compression design (LLDC) is proposed for the wearable devices. The electrocardiogram (ECG), blood pressure (BP), and respiration (RESP) can be applied to the compression design for cardiovascular diseases. The proposed LLDC can detect the abnormal symptoms and dynamically change the compression modes with different sample intervals and data precisions. In our experiments, the symptoms are detected, and the transmitted power and temperature for the wearable devices are reduced. The compression ratios for ECG, BP, and RESP are up to 7.94, 6.06, and 6.51 with percentage root-mean-square difference less than 6.5%. For ECG, BP, and RESP, the energies of the wearable devices are reduced by 50%-87%, 38%-89%, and 41%-89%; the temperatures are reduced by 2.6 °C-4.2 °C, 1.3 °C-3 °C, and 1.7 °C-3.6 °C, respectively.

5)Exploiting similar prior knowledge for compressing ECG signals

Data compression techniques have been used in order to reduce power consumption when transmitting electrocardiogram (ECG) signals in wireless body area networks (WBAN). Among these techniques, compressed sensing allows sparse or compressible signals to be encoded with only a small number of measurements. Although ECG signals are not sparse, they can be made sparse in another domain. Numerous sparsifying techniques are available, but when signal

quality and energy consumption are important, existing techniques leave room for improvements.

6) A 3-Lead ECG-on-Chip with QRS Detection and Lossless Compression for Wireless Sensors

This brief presents the design of a low-power 3-lead electrocardiogram (ECG)-on-chip with integrated real-time QRS detection and lossless data compression for wearable wireless ECG sensors. Data compression and QRS detection can reduce the sensor power by up to 2-5 times. A joint QRS detection and lossless data compression circuit allows computational resources to be shared among multiple functions, thus lowering the overall system power. The proposed technique achieves an average compression ratio of 2.15 times on standard test data. The QRS detector achieves a sensitivity (Se) of 99.58% and positive productivity (+P) of 99.57% @ 256 Hz when tested with the MIT/BIH database. Implemented in 0.35 µm process, the circuit consumes 0.96 µW @ 2.4 V with a core area of 1.56 mm^2 for two-channel ECG compression and QRS detection. Small size and ultralow-power consumption makes the chip suitable for usage in wearable/ambulatory ECG sensors.

PROPOSED SYSTEM

In the proposed approach, first-order derivative D(n) is initially evaluated from the successive digitized ECG samples, i.e., current sample value and previous sample value. The calculated D(n) are mostly centralized around zero. It demonstrates the histogram of D(n) values for ten ECG signals from MIT-BIH database, each of 1 min duration. However, in certain regions, a typical ECG signal consists of variations in amplitude corresponding to peaks, such as P-wave, R-peak, and T-wave. Due to this amplitude variation, the D(n) values are different for different regions. The proposed algorithm has been tested with digitized input ECG signal with and without preprocessing. The calculated mean of each packet is then compared with the three predefined threshold values, which are calculated considering possible maximum of the |D(n)| samples corresponding to three different regions, i.e., low-amplitude region, medium-amplitude region, and high-amplitude region where th3 > th2 > th1. Based on the range of M, three different divisors are selected as shown in Fig. 3.1. The generated bitstreamD1(n) is then sent to the encoder that produces compressed bitstream Dc (n).

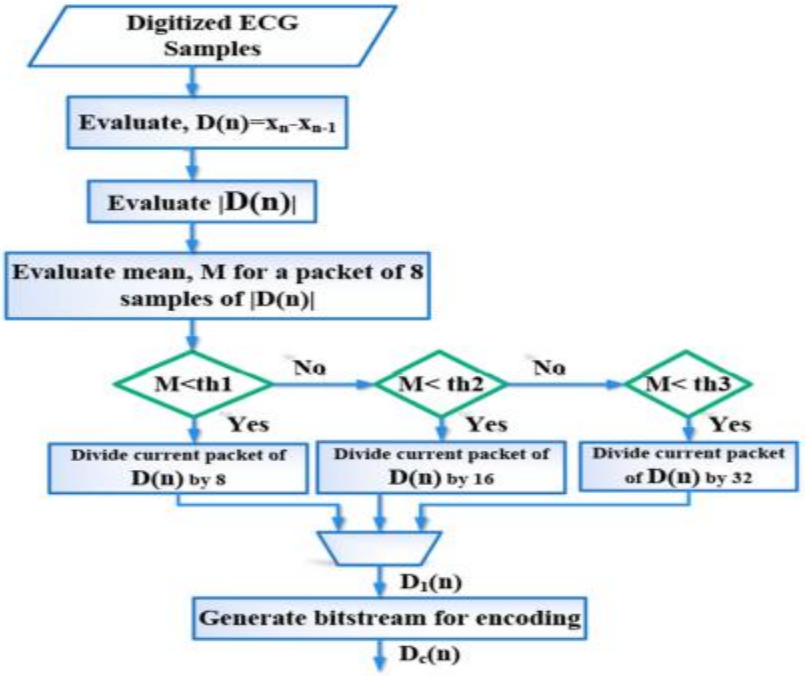


Figure 1.Flowchart of proposed lossless compression scheme

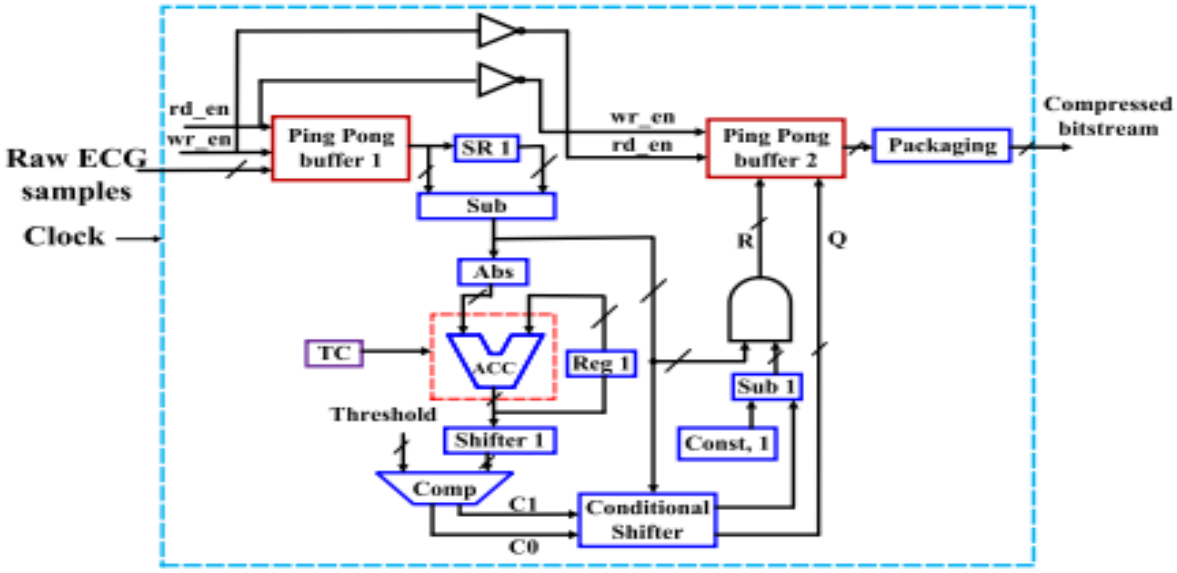


Figure 2 Block Diagram of the Hardware Architecture

The hardware implementation of the proposed algorithm is discussed in this section. The block-level representation of the proposed architecture is shown in Fig. 3.3. It demonstrates the generation of compressed data from the ECG samples followed by data packaging. The digitized input data stream consists of 11 bits/sample. Ping pong buffers of size 11 × 8 are used for storing the packets.

A “written” and “red signal” signals enable to write in the buffers and read the buffers, respectively. Initially, the data are fetched through a shift register (SR 1), which is eventually subtracted as mentioned in (1) by the “sub" block, producing first-order derivative, i.e., D(n). In order to select the appropriate divisor k, the mean of eight samples is calculated from the absolute values of the D(n). “Abs” block produces the absolute values of D(n) using 2’s complement technique.

The values are added in the accumulator “ACC,” which is controlled by a terminal counter TC. TC is used for extracting the output after the addition of eight samples in each packet. Right shifting the corresponding output by “Shifter 1” generates the mean value of the current packet. The obtained mean is compared with the “Comp” block with predefined threshold values (th1, th2, and th3), producing control signalsC0 and C1. Based on the combinations of C0 and C1, D(n) are shifted right by the conditional shifter to get quotient value Q. The conditional shifter also includes a left shift module, which generates logic values of 8, 16, and 32 by left shifting a constant value “2”, depending on the control signals C0 and C1. The condition “C0C1=00” denotes no left or right shift. A subtractor “sub 1” is used for subtracting constant 1 from the logic value generated from the left shift module.

The D(n) value is logically added with “sub 1” output, resulting in the remainder R. The obtained values are sent for packaging and then transmitted to the remote server. In order to minimize complex operations, the proposed architecture is designed based on first derivative operations and sub modules are implemented with subtractor, shifter, counters, and comparators.

PROPOSED MULTI-LEVEL ECG COMPRESSION ARCHITECTURE

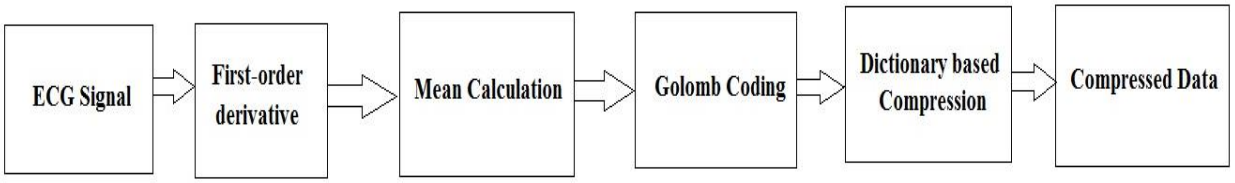


Figure 3 Proposed block diagram

RUN-LENGTH ENCODING

Run-length encoding (RLE) is a form of lossless data compression in which runs of data (sequences in which the same data value occurs in many consecutive data elements) are stored as a single data value and count, rather than as the original run. This is most efficient on data that contains many such runs, for example, simple graphic images such as icons, line drawings, Conway's Game of Life, and animations. For files that do not have many runs, RLE could increase the file size.

Consider a screen containing plain black text on a solid white background. There will be many long runs of white pixels in the blank space, and many short runs of black pixels within the text. A hypothetical scan line, with B representing a black pixel and W representing white, might read as follows:

WWWWWWWWWWWWBWWWWWWWWWWWWWWBBBWWWWWWWWWWWWWWWWWWWW
WWWWWWWWBWWWWWWWWWWWWWW

With a run-length encoding (RLE) data compression algorithm applied to the above hypothetical scan line, it can be rendered as follows:

12W1B12W3B24W1B14W

This can be interpreted as a sequence of twelve Ws, one B, twelve Ws, three Bs, etc., and represents the original 67 characters in only 18. While the actual format used for the storage of

images is generally binary rather than ASCII characters like this, the principle remains the same. Even binary data files can be compressed with this method; file format specifications often dictate repeated bytes in files as padding space. However, newer compression methods such as DEFLATE often use LZ77-based algorithms, a generalization of run-length encoding that can take advantage of runs of strings of characters (such as `BWWBWWBWWBWW`).

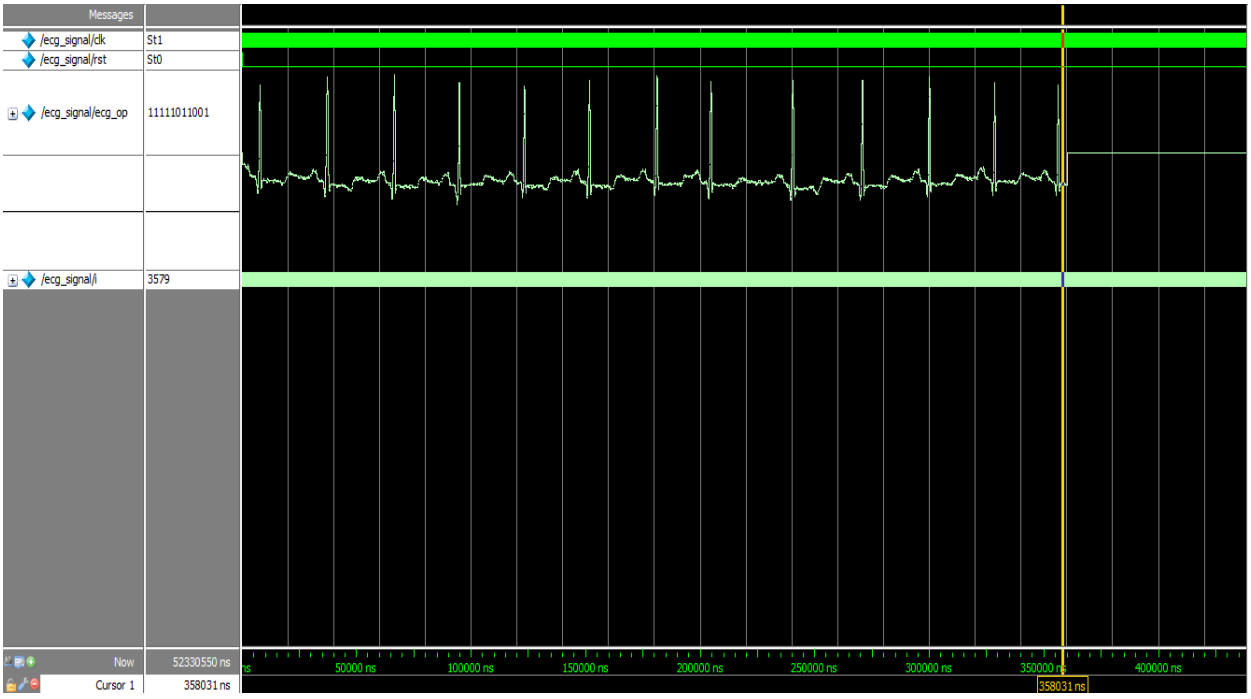
Run-length encoding can be expressed in multiple ways to accommodate data properties as well as additional compression algorithms. For instance, one popular method encodes run lengths for runs of two or more characters only, using an "escape" symbol to identify runs, or using the character itself as the escape, so that any time a character appears twice it denotes a run. On the previous example, this would give the following:

WW12BWW12BB3WW24BWW14

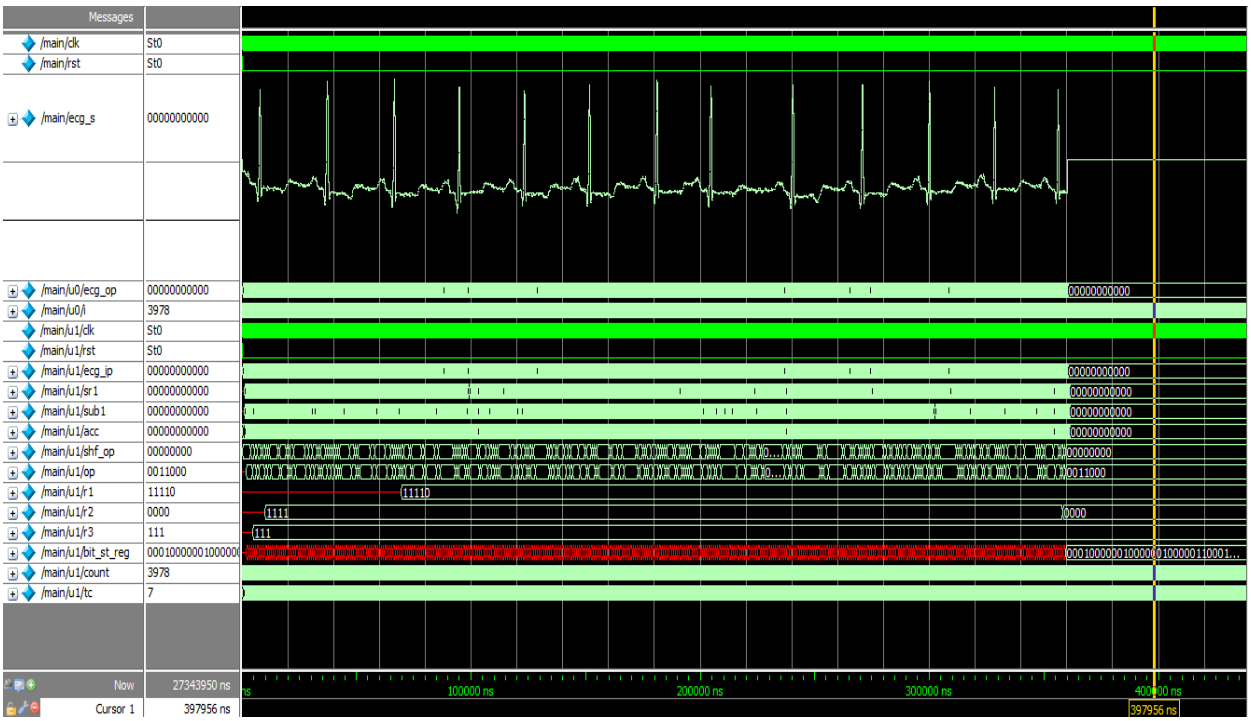
This would be interpreted as a run of twelve Ws, a B, a run of twelve Ws, a run of three Bs, etc. In data where runs are less frequent, this can significantly improve the compression rate.

RESULTS

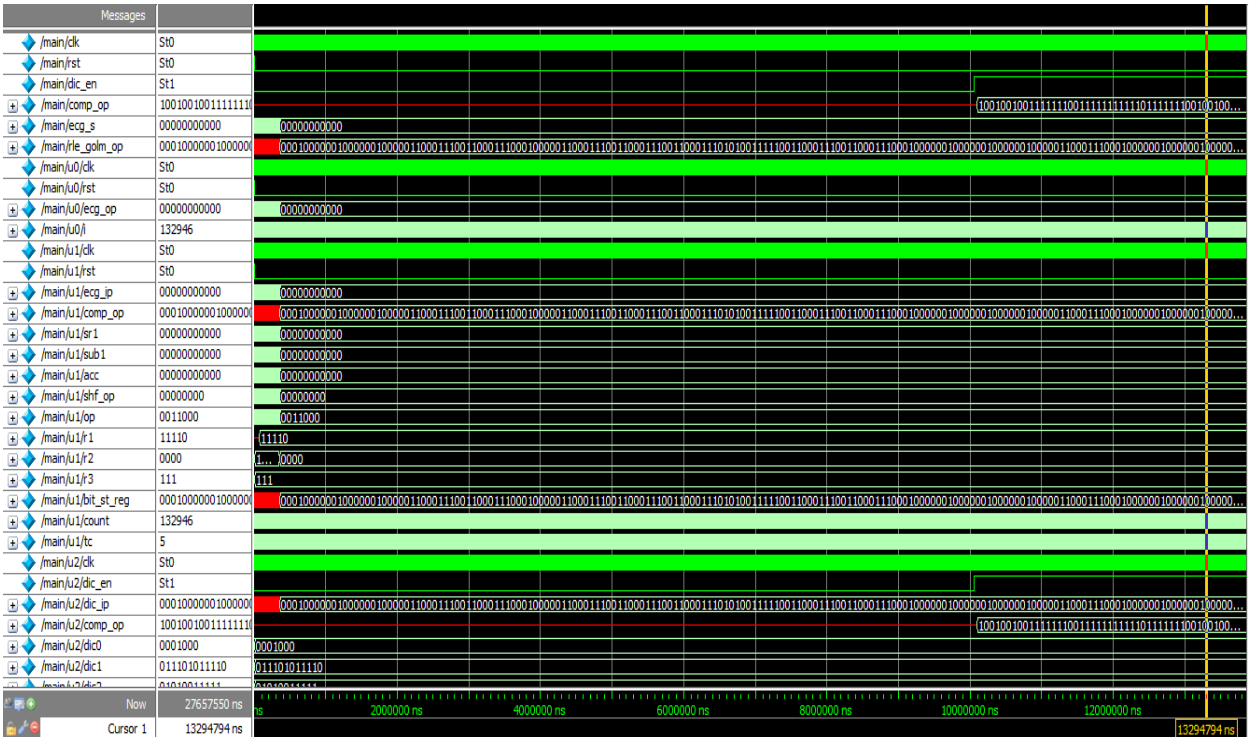
SIMULATION RESULT OF INPUT ECG SIGNAL



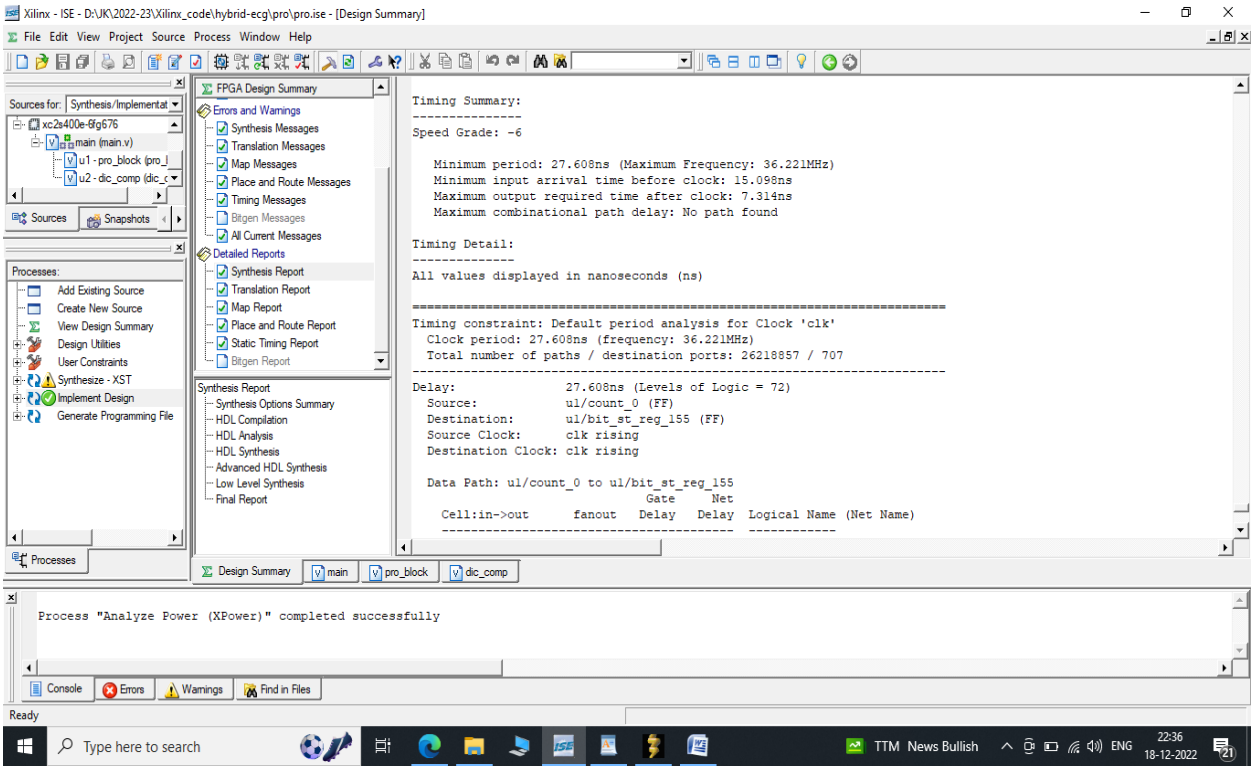
SIMULATION RESULT OF EXISTING METHOD



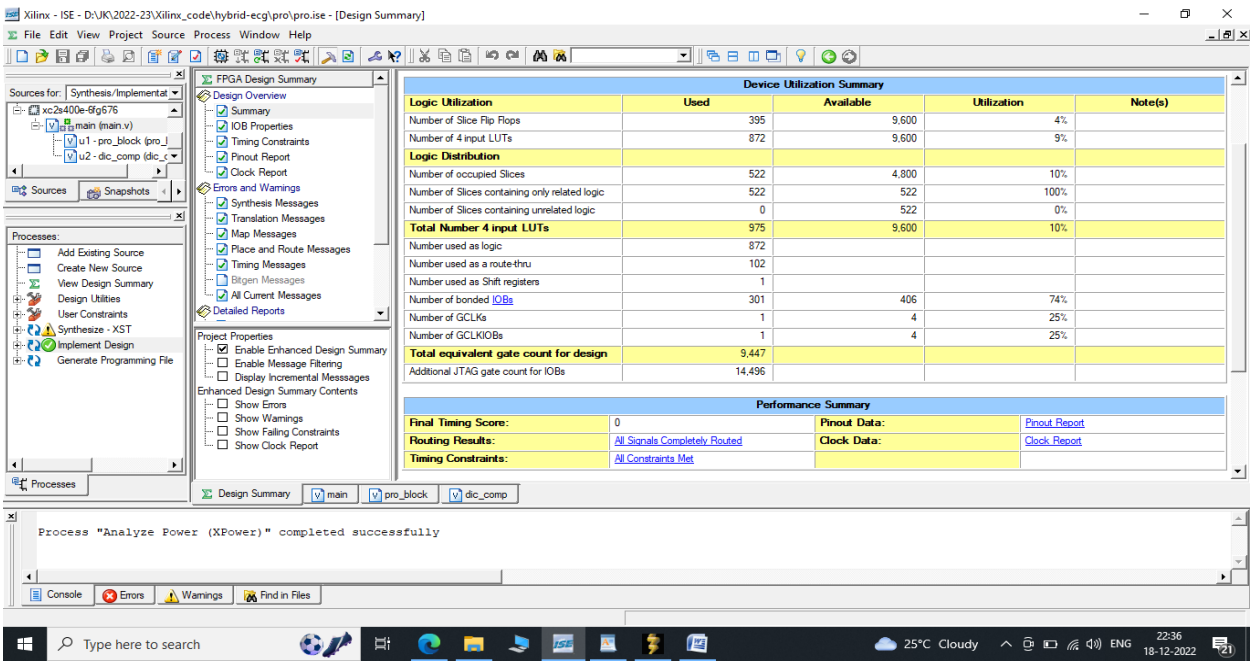
SIMULATION RESULT OF PROPOSED METHOD



DELAY REPORT OF PROPOSED METHOD



AREA REPORT OF PROPOSED METHOD



CONCLUSION

Theproposed work demonstrates an on-node hybrid lossless ECG compression architecture for sensor nodes that can improve CR. The proposed compression scheme is compatible in sensor node, achieving good CR. Further, multi-level compression scheme based on runlength, golomb and dictionary selection helps in achieving efficient compression. The proposed architecture consumes low powerpower at 100 MHz operating frequency. Nominal power consumption and area overhead with maximum operating frequency of 250 MHz make the proposed architecture compatible in miniaturized sensor nodes. Besides, 6% of the transmission power has been saved in this transmission mode over uncompressed ECG for a transmission period of 1 min. The proposed scheme can be further stretched for other biomedical signals.

REFERENCES

[1] F. Nasimi, M. R. Khayyambashi, N. Movahhedinia, and Y. W. Law, "Exploiting similar prior knowledge for compressing ECG signals," Biomed. Sig. Proc. Control, vol. 60, 2020, Art. no. 101960.

[2] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 µw analog signal processor ASIC for portable biopotential signal monitoring," IEEE J. Solid-State Circuits, vol. 46, no. 1, pp. 209–223, Jan. 2011.

[3] C. J. Deepu, X. Zhang, C. H. Heng, and Y. Lian, "A 3-lead ECG-on-Chip with QRS detection and lossless compression for wireless sensors," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 63, no. 12, pp. 1151–1155, Dec. 2016.

[4] S.-L. Chen and J.-G.Wang, "VLSI implementation of low-power cost-efficient lossless ECG encoder design for wireless healthcare monitoring application," Electron.Lett., vol. 49, no. 2, pp. 91–93, 2013.

[5] S.-Y. Lin, H.-T.Lin, and Y.-Y. Lin, "Lossless and lossy direct compression design with multi-signal symptom detection for low-temperature wearable devices," IEEE Sensors J., vol. 19, no. 2, pp. 715–725, Jan. 2019.

[6] C.-H. Luo et al., "An ECG acquisition system prototype design with flexible PDMS dry electrodes and variable transform length DCT-IV based compression algorithm," IEEE Sensors J., vol. 16, no. 23, pp. 8244–8254, Dec. 2016.

[7] Y. Yin et al., "A 2.63 µw ECG processor with adaptive arrhythmia detection and data compression for implantable cardiac monitoring device," IEEE Trans. Biomed. Circuits Syst., vol. 15, no. 4, pp. 777–790, Aug. 2021.

[8] J. Ma, T. Zhang, and M. Dong, "A novel ECG data compression method using adaptive fourier decomposition with security guarantee in e-health applications," IEEE J. Biomed. Health Informat., vol. 19, no. 3, pp. 986–994, May 2015.

[9] T.-H. Tsai, N.-C.Tung, and D.-B. Lin, “VLSI implementation of multi-channel ECG lossless compression system,” IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 68, no. 8, pp. 2962–2966, Aug. 2021.
[10] K. Li, Y. Pan, F. Chen, K.-T. Cheng, and R. Huan, “Real-time lossless ECG compression for low-power wearable medical devices based on adaptive region prediction,” Electron.Lett., vol. 50, no. 25, pp. 1904–1906, 2015.
[11] T.-H. Tsai and M. A. Hussain, “VLSI implementation of lossless ECG compression algorithm for low power devices,” IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 67, no. 12, pp. 3317–3321, Dec. 2020.
[12] N. Attarmoghaddam, S. H. Khayat, and M. Maymandi-Nejad, “FPGA implementation of power and area efficient compressed sensing for multi-channel ECG compression,” in Proc. 24th Iranian Conf. Elect. Eng., 2016, pp. 1027–1032.
[13] Rajagopal, R., Karthick, R., Meenalochini, P., & Kalaichelvi, T. (2023). Deep Convolutional Spiking Neural Network optimized with Arithmetic optimization algorithm for lung disease detection using chest X-ray images. Biomedical Signal Processing and Control, 79, 104197.
[14] Srinivas, T. Aditya Sai, B. Ravindra Babu, Miskir Solomon Tsige, R. Rajagopal, S. Devi, and Subrata Chowdhury. "Effective implementation of the Prototype of a digital stethoscope using a Smartphone." In 2022 International Conference on Innovative Computing, Intelligent Communication and Smart Electrical Systems (ICSES), pp. 1-8. IEEE, 2022.
[15] Rajagopal, R., M. Karthik, M. Soni, Narayan Krishan Vyas, S. Hemavathi, and M. R. Arun. "Monitoring the high-speed engine application using ferro magnetic system." Materials Today: Proceedings (2022).
[16] Babu, P. Ramesh, Vemuri Kusuma Priya, N. Drawin, R. Thiagarajan, and R. Krishnamoorthy. "Enhanced Hybrid Resource Scheduler for an Institution Employing NB-RR Scheduling." In 2022 8th International Conference on Smart Structures and Systems (ICSSS), pp. 1-6. IEEE, 2022.
[17] Jose, S. Edwin, R. Lal Raja Singh, and R. Rajagopal. "Automatic and real time classification of power quality disturbance using statistical moments." AIP Conference Proceedings. Vol. 2327. No. 1. AIP Publishing LLC, 2021.
[18] Rajagopal, R., and S. Edwin Jose. "An Efficient Framework for Locating Stroke in Brain MRI Images Using Radon Transform and Convolutional Neural Networks." In Next Generation of Internet of Things, pp. 385-395. Springer, Singapore, 2021.
[19] Rajagopal, R., and P. Subbaiah. "A survey on liver tumor detection and segmentation methods." ARPN Journal of Engineering and Applied Sciences 10, no. 6 (2015): 2681-2685
[20] Rajagopal, R., & Subbiah, P. (2014). Computer aided detection of liver tumor using SVM classifier. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 3(6), 10170-7.
[21] Rajagopal, R. (2019). Glioma brain tumor detection and segmentation using weighting random forest classifier with optimized ant colony features. International Journal of imaging systems and technology, 29(3), 353-359.