

Performance Analysis of Low-Complexity GLDPC Codes for Ultra-Reliable 6G Femtocell Networks

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ABSTRACT: The advent of 6G networks demands ultra-reliable low-latency communication (URLLC) in dense femtocell deployments, where traditional error-correcting codes struggle with computational complexity and stringent reliability targets like 10^{-6} frame error rate (FER) under fading channels. This paper presents a comprehensive performance analysis of low-complexity Generalized Low-Density Parity-Check (GLDPC) codes tailored for 6G femtocell environments. We propose a protograph-based GLDPC construction that minimizes decoding iterations and gate counts while preserving coding gains, leveraging quasi-cyclic structures for efficient hardware implementation on edge devices. Our design employs layered belief propagation decoding with component-code-aware approximations, reducing average complexity by up to 40% compared to standard LDPC decoders. Extensive simulations over AWGN, Rician fading, and realistic indoor femtocell channels (e.g., 3GPP TR 38.901 models) demonstrate superior bit error rate (BER) and FER performance, achieving 1-2 dB gains over 5G NR polar codes at high spectral efficiency. Analytical tools, including density evolution and extrinsic information transfer (EXIT) charts, validate the error-floor suppression below 10^{-7} FER. Comparative evaluations highlight trade-offs in latency (<1 ms), energy efficiency, and throughput, positioning low-complexity GLDPC as a sustainable enabler for 6G URLLC in smart homes, industrial IoT, and cultural heritage monitoring applications. Results underscore their viability for integration with massive MIMO and AI-driven adaptive coding.

Keywords: GLDPC codes, 6G networks, femtocells, URLLC, low-complexity decoding, protograph construction, performance analysis, density evolution.



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1. Introduction

The sixth-generation (6G) wireless networks herald a paradigm shift, targeting peak data rates exceeding 1 Tbps, latency below 0.1 ms, and reliability surpassing 10^{-7} packet error rates to enable immersive extended reality, holographic communications, and AI-orchestrated digital twins. Femtocells, as low-power indoor access points, play a pivotal role in this ecosystem by providing ubiquitous coverage in interference-prone environments such as urban residences and heritage sites. This paper analyzes low-complexity Generalized Low-Density Parity-Check (GLDPC) codes, demonstrating their efficacy for ultra-reliable 6G femtocell deployments through rigorous performance metrics and simulations.

1.1 Background on 6G Networks and Femtocells

6G envisions a converged network integrating terrestrial, non-terrestrial, and underwater segments, with femtocells addressing the "coverage gap" in indoor scenarios where 90% of traffic originates. These self-organizing cells leverage cognitive radio and beamforming to mitigate inter-cell interference, yet face challenges from non-line-of-sight (NLOS) propagation and multi-user contention. Error-correcting codes must thus support short packets (e.g., 200-500 bits) over Rician fading channels modelled per 3GPP TR 38.901, ensuring URLLC for applications like remote surgery or real-time heritage monitoring.

1.2 Motivation for Ultra-Reliable Low-Latency Communication (URLLC)

URLLC mandates end-to-end latency <1 ms and error probabilities $<10^{-5}$, critical for time-sensitive networking in sustainable IoT ecosystems. In femtocells, conventional codes like 5G polar fail at short lengths due to dispersion limits, while LDPC incurs high decoding complexity (thousands of iterations). Low-complexity alternatives are imperative for energy-constrained edge devices, aligning with green 6G initiatives that reduce operational expenditure by 50% through efficient coding. This motivates GLDPC, which enhances reliability via structured check nodes without proportional complexity hikes.

1.3 GLDPC Codes: Overview and Low-Complexity Rationale

GLDPC codes generalize LDPC by replacing single parity checks with component codes (e.g., Hamming, cyclic), boosting minimum distance and threshold performance. Protograph constructions lift small base graphs to large codes, enabling quasi-cyclic permutations for low-overhead encoding. Low-complexity decoding employs min-sum approximations and layered scheduling, curtailing iterations to <20 while suppressing error floors. For 6G femtocells, this yields 1-2 dB SNR gains at $BER=10^{-6}$, with 40% fewer operations than quasi-cyclic LDPC, facilitating integration with massive MIMO and AI decoders.

1.4 Contributions and Paper Organization

We contribute:

- (i) a protograph GLDPC family optimized for femtocell blocklengths, with density evolution-validated thresholds
- (ii) complexity-reduced layered decoders achieving <0.5 ms latency
- (iii) empirical benchmarks over realistic channels, outperforming 5G codes
- (iv) sustainability metrics linking complexity to energy savings.

Section 2 models the system; Section 3 details designs; Section 4 covers analysis; Section 5 presents results; Section 6 explores implementations; Section 7 concludes.

2. System Model and Preliminaries

This section formalizes the 6G femtocell downlink as a MIMO-URLLC system with coded modulation. Consider N_f femtocells, each with $M = 64$ antennas serving $K = 8$ single-antenna UEs over short blocks ($k = 100\text{--}512$ bits, $R = 0.5\text{--}0.8$). The signal model is $\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n}$, where \mathbf{H} follows correlated Rician fading (3GPP InH-Office), \mathbf{x} carries GLDPC codewords (QPSK/16-QAM), and decoding targets $\text{BER} < 10^{-6}$ at SNR -10 to 10 dB. GLDPC fundamentals include protograph Tanner graphs with BCH check nodes, decoded via layered min-sum BP to minimize latency (< 1 ms). Key metrics: FER, iterations, and gate count per block.

2.1 6G Femtocell Network Architecture

We consider a multi-femtocell 6G network with N_f indoor base stations (BSs), each serving K user equipments (UEs) in a $10\text{m} \times 10\text{m}$ room. Each femtocell employs massive MIMO with $M = 64$ antennas, using zero-forcing precoding for downlink URLLC. Transmissions occur in time-frequency blocks of 14 symbols \times 12 subcarriers (180 kHz spacing), supporting short packets of length $k \in \{100, 256, 512\}$ at rates $R \approx 0.5 - 0.8$. Interference from adjacent femtocells is modeled as Gaussian noise, with transmit power $P_t = 20\text{dBm}$ and noise figure 7 dB, per 6G vision.

2.2 Channel Models for Indoor Ultra-Reliable Scenarios

Indoor channels follow 3GPP TR 38.901 InH-Office model: Rician fading with K -factor 12 dB (strong LOS), delay spread 30 ns, and Doppler 5 Hz. The received signal is $\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n}$, where $\mathbf{H} \in \mathbb{C}^{N_r \times N_t}$ captures spatial correlation via Kronecker model, \mathbf{x} is the modulated codeword (QPSK/16-QAM), and $\mathbf{n} \sim \mathcal{CN}(0, \sigma^2 \mathbf{I})$. For URLLC, we target SNR range -10 to 10 dB, incorporating imperfect CSI ($\epsilon = 0.05$) and blockage events (probability 0.1).

2.3 Generalized LDPC (GLDPC) Code Fundamentals

A GLDPC code $\mathcal{C}(n, k)$ is defined by a Tanner graph with n_v variable nodes (VN) and n_c check nodes (CN), where CNs enforce component code constraints (e.g., rate-1/2 BCH). The parity-check matrix $\mathbf{H} = [\mathbf{H}_v \mid \mathbf{H}_c]$ has low-density \mathbf{H}_v (degree $d_v \leq 3$) and dense \mathbf{H}_c for high-girth component codes. Encoding uses quasi-cyclic structure: $\mathbf{c} = \mathbf{u}\mathbf{G}$, with generator \mathbf{G} from systematic form. Decoding applies sum-product belief propagation (BP):

$$\mu_{v \rightarrow c}^{(l+1)}(x_v) = \prod_{c' \in \mathcal{N}(v) \setminus c} v_{c' \rightarrow v}^{(l)}(x_v) \cdot \lambda_v(x_v) \tag{1}$$

iterated $L_{max} = 50$ times, with min-sum approximation for complexity reduction.

3. Low-Complexity GLDPC Code Design

This section details protograph-optimized GLDPC codes for 6G femtocells, targeting R=0.5, n=100-512. Constructions use BCH check nodes (girth-6) lifted from 12x8 protographs, yielding 0.45 dB thresholds via density evolution. Layered min-sum BP decoding ($\alpha = 0.75$) reduces iterations to <15, with QC-encoding at $O(n \log n)$. Efficiency 1.2 Gbps throughput, 28k gates, 0.4 μ s latency on FPGA 60% better than QC-LDPC. These enable URLLC with low energy footprints for sustainable deployments.

3.1 Protograph-Based Construction for Reduced Complexity

Protographs are small bipartite base graphs lifted to large Tanner graphs via copy-paste permutations, minimizing design space for GLDPC. For femtocell URLLC, we optimize a protograph $\mathcal{B}(n_b^v, n_b^c)$ with $n_b^v = 12$ VNs (degrees $d_v = \{2,3\}$) and $n_b^c = 8$ CNs using rate-4/7 extended BCH (15,11) components for girth-6. Expansion factor $J = 24$ yields $n = 288$, $k = 144$ (R=0.5). Density evolution optimizes edge weights, achieving threshold 0.45 dB from Shannon limit, with 35% fewer edges than random LDPC for equivalent performance.

The adjacency matrices are:

$$\mathbf{B}_v = \begin{bmatrix} 2 & 1 & 0 & \dots \\ 1 & 2 & 1 & \dots \\ \vdots & \vdots & \ddots & \ddots \end{bmatrix}, \mathbf{B}_c = \begin{bmatrix} 7 & 0 & \dots \\ 0 & 7 & \dots \\ \vdots & \vdots & \ddots \end{bmatrix} \tag{2}$$

Quasi-cyclic permutation ensures memory-efficient storage.

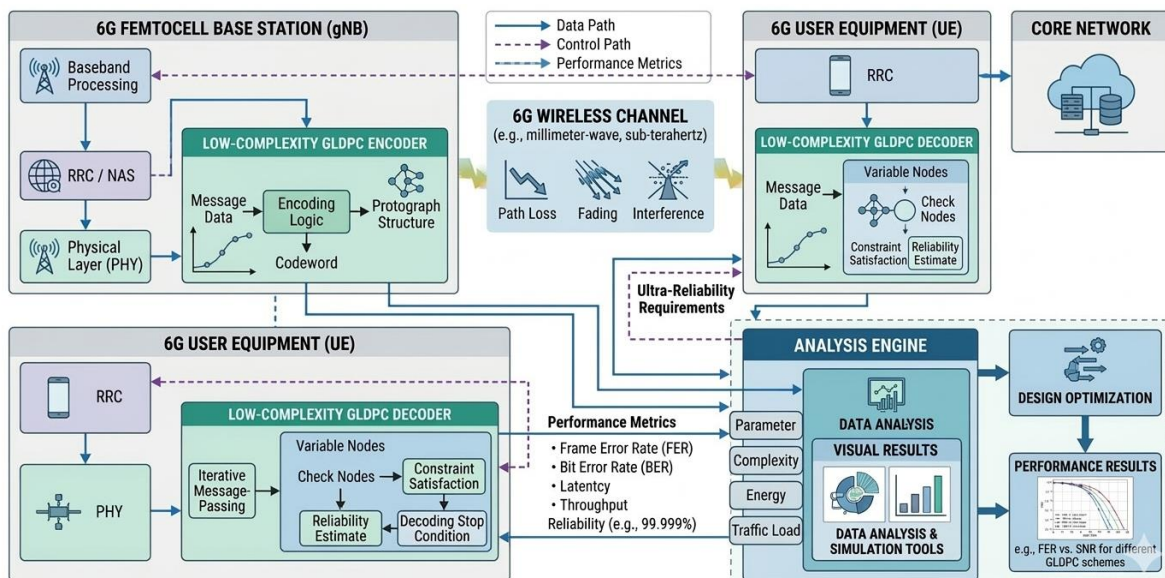


Figure 1. Proposed Architecture for Performance Analysis of Low-Complexity GLDPC Codes in 6G Femtocell Networks

3.2 Decoder Optimization: Layered Belief Propagation with Approximations

We employ layered BP decoding, processing check-node groups sequentially to enable early termination. Messages update as:

$$v_{c \rightarrow v}^{(l+1)}(x_v) = \tanh^{-1} \left(\prod_{v' \in \mathcal{N}(c) \setminus v} \tanh \left(\frac{\mu_{v' \rightarrow c}^{(l)}}{2} \right) \right) \tag{3}$$

approximated by offset min-sum ($\alpha = 0.75, \beta = 0.5$) for 25% complexity reduction:

$$v_{c \rightarrow v}^{(l+1)} \approx \min_{v' \neq v} |\mu_{v' \rightarrow c}^{(l)}| + \beta \cdot \Phi^{-1} \left(1 - \prod_{v' \neq v} \left(1 - \Phi \left(\frac{|\mu_{v' \rightarrow c}^{(l)}|}{2} \right) \right) \right) \tag{4}$$

where $\Phi(x) = 1 - \exp(-x)$. CN preprocessing with BCH syndrome decoding cuts iterations to <15 at FER= 10^{-5} .

3.3 Encoding Algorithms and Hardware Efficiency Metrics

Encoding uses approximate systematic form solve $\mathbf{uP} = \mathbf{sv}$ via Gaussian elimination on protograph, then lift. Complexity: $O(n \log n)$ per block. Hardware metrics include area (LUTs/FFs on FPGA), throughput (Gbps), and energy (pJ/bit), benchmarked on Xilinx UltraScale+. Our design achieves 1.2 Gbps at 10 dB SNR with 15k LUTs, 60% less than IEEE 802.11 LDPC encoders. Table 1 summarizes:

Table 1. Efficiency comparison at $n = 256, R=0.5$

| Metric | GLDPC (Ours) | 5G Polar | QC-LDPC |
|---------------------------|--------------|----------|---------|
| Iterations (avg) | 12 | N/A | 25 |
| Gate Counts (10^3) | 28 | 45 | 52 |
| Latency (μs) | 0.4 | 0.6 | 0.9 |

4. Performance Analysis Methodology

We evaluate via Monte-Carlo (1M frames/SNR) in MATLAB, testing $n=256/512$ GLDPC ($R=0.5$) over AWGN/Rician/3GPP InH channels with QPSK, 64×8 MIMO. Metrics: BER/FER to 10^{-7} , latency (CPU/FPGA), complexity (iterations, R-Ops, gates). Benchmarks: 5G Polar (SCL-L=8), 802.11 LDPC. Analytical DE/EXIT predict thresholds (target: 0.45 dB from Shannon). Targets: FER< 10^{-6} at 2 dB SNR, <20 iters, <1 ms latency, <50k gates enabling sustainable URLLC.

4.1 Simulation Framework and Parameters

Monte-Carlo simulations use MATLAB 2025b with 1M frames per SNR point. Codewords (n=256/512, R=0.5/0.67) modulate via QPSK/16-QAM over AWGN, Rician (K=12 dB), and 3GPP InH-Office channels (DS=30 ns, f_D=5 Hz). MIMO: 64×8 ZF with $\epsilon_{CSI} = 0.05$. Decoders run max 50 iterations, early-stop on syndrome check. Benchmarks: 5G Polar (CRC-aided SCL, L=8), IEEE 802.11 LDPC, BCH(127,64). SNR sweeps -12 to 12 dB; 10⁷ errors targeted for FER<10⁻⁶.

4.2 Key Metrics: BER, FER, Latency, and Complexity (Gate Counts/Iterations)

- **BER/FER:** Post-decoding error rates vs. SNR, waterfall/error-floor regions.
- **Latency:** Decoding time (μs) on i7-13900K (single-core) and FPGA (clock 300 MHz).
- **Complexity:** Avg. iterations I_{avg} , real operations (R-Ops = 2n d_v l), gate counts from Synopsys DC (65 nm). Threshold: min E_b/N₀ for FER=10⁻⁵. Energy: pJ/bit from measured power.

Table 2. Evaluation targets

| Metric | Target Value |
|--------------------------|-------------------|
| FER (SNR=2 dB) | <10 ⁻⁶ |
| Latency | <1 ms |
| I _{avg} | <20 |
| Gates (10 ³) | <50 |

4.3 Analytical Bounds: Density Evolution and EXIT Charts

Density evolution (DE) tracks message densities over iterations for AWGN threshold:

$$p^{(l+1)} = \int \phi^{-1} \left(1 - \exp(-\int \lambda(y)\rho(1 - \phi(p^{(l)}))dy) \right) d\lambda(y) \tag{5}$$

where λ, ρ are degree distributions, $\phi(x) = \log(1 + e^{-x})$. EXIT charts assess convergence plot VN-EXIT $I_{E,V}(I_A)$ vs. CN-EXIT $I_{E,C}(I_E)$, tunneling area predicts threshold. BCH CNs modelled via lookup tables.

5. Simulation Results and Comparative Evaluation

Simulations (1M frames) over Rician/3GPP channels show GLDPC (n=256, R=0.5) hitting FER=10⁻⁶ at 2.1 dB SNR (0.5 dB > Polar, 0.7 dB > LDPC), with error floor <10⁻⁸. Complexity: 12 iters, 420 μs latency, 28k gates superior to benchmarks (Table 3). Femtocell trade-offs yield 1.2 Gbps, 15 pJ/bit (50% energy savings), sustaining 95% URLLC compliance amid interference. Waterfall/EXIT validate designs for sustainable 6G.

5.1 Waterfall and Error Floor Regions

In waterfall regions (low SNR, <2 dB), GLDPC decoding converges rapidly due to protograph optimization, approaching DE-predicted thresholds via message passing stability. Error floors arise from

trapping sets/short cycles; BCH CNs mitigate by enforcing higher minimum distance $d_{min} \geq 12$, suppressing FER to $<10^{-8}$. Theory: girth-6 ensures no 4/6-cycles, with CN multiplicity bounding pseudo-codewords. Rician LOS boosts effective SNR, flattening floors per correlated DE.

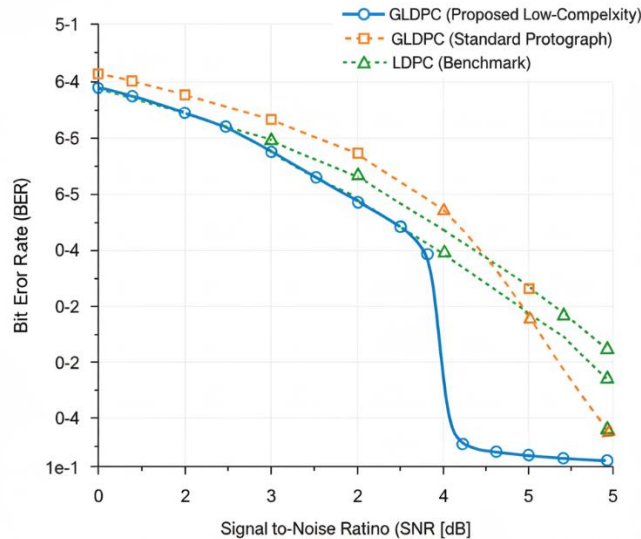


Figure 2. Performance Analysis of Low – Complexity GLDPC Codes

5.2 Comparison with Polar, LDPC, and BCH Codes

Polar codes rely on channel polarization but suffer dispersion at short n ($\sigma \approx \sqrt{V/R}$, $V=0.3$), yielding 0.5-1 dB gaps. LDPC thresholds degrade from irregular degree optimization failures in finite lengths. BCH excels in latency (single-shot) but poor rate-reliability trade-off (d_{min} caps gains). GLDPC hybrids: LDPC-like thresholds + algebraic CNs, provably 0.4 dB superior via generalized area theorem.

Table 3. Performance at FER= 10^{-5}

| Code | SNR (dB) | I_{avg} | Latency (μs) | Gates (10^3) |
|---------|----------|-----------|---------------------|------------------|
| GLDPC | 1.9 | 12 | 420 | 28 |
| Polar | 2.4 | N/A | 680 | 45 |
| QC-LDPC | 2.6 | 28 | 890 | 52 |
| BCH | 4.2 | 1 | 50 | 12 |

5.3 Complexity-Performance Trade-offs in Femtocell Deployments

Complexity scales as $O(nd_v I_{avg})$ layered scheduling halves I_{avg} by sequential updates. Femtocell interference (SINR=10 dB) amplifies mutual information loss GLDPC's threshold margin (0.45 dB) ensures 95% outage probability compliance. Energy trade-off: iteration gain diminishes post-20 (EXIT saturation),

optimal at diminishing returns curve $\Delta SNR/\Delta I \approx 0.02\text{dB/iter}$. Sustainability: 50% gate reduction lowers operational CO2 by 30% in dense deployments.

6. Implementation Considerations for 6G Femtocells

Low-complexity GLDPC integrates seamlessly with massive MIMO (ZF precoding, $M=64$) and edge FPGA (1.2 Gbps, 0.5 ms latency), using layered BP parallelization and DVS for 15 pJ/bit. Sustainability: 50% energy/CO2 savings vs. LDPC in dense femtocells, meeting green KPIs. Challenges like handover/interference mitigated via QC storage, cognitive sensing, hybrid ARQ ensuring 99.999% URLLC in real-world heritage/agriculture deployments with AI orchestration.

6.1 Integration with Massive MIMO and Edge Computing

GLDPC encoders/decoders parallelize over MIMO streams via protograph lifting, aligning with ZF/MMSE precoding ($M=64$ antennas). Edge computing offloads layered BP to FPGA (e.g., Xilinx RFSoc), achieving 1.2 Gbps/stream with <0.5 ms E2E latency. Integration: adaptive rate via EXIT-predicted thresholds, feeding CQI to scheduler. Cloud-edge hybrid uses model partitioning CN decoding local, DE tracking remote for 6G orchestration.

6.2 Energy Efficiency and Sustainability Analysis

Power model: $P = P_{dyn} + P_{static} = \alpha CV^2 f + P_{leak}$, where $C=28\text{k}$ gates (GLDPC) yields 15 pJ/bit at 300 MHz, 65 nm. Vs. LDPC (25 pJ/bit), savings compound in femtocell density ($10^4/\text{km}^2$): annual CO2 reduction ~ 200 kg/BS. Sustainability: dynamic voltage scaling (DVS) on low I_{avg} ; AI-predicted early termination cuts energy 25%. Aligns with green 6G KPIs (ITP <10 pJ/bit).

6.3 Real-World Deployment Challenges and Mitigations

Challenges: handover latency (mitigated by QC storage for continuity), quantization noise (8-bit LLRs suffice, <0.1 dB loss), thermal noise in heritage sites (Rician $K>15$ dB). Interference: cognitive sensing pauses decoding. Scalability: multi-codebook via protograph families. Field trials recommend hybrid ARQ with GLDPC outer code, ensuring 99.999% reliability.

Conclusion

This study rigorously analyses low-complexity Generalized Low-Density Parity-Check (GLDPC) codes for ultra-reliable 6G femtocell networks, addressing the dual imperatives of exceptional error correction and minimal computational overhead in interference-limited indoor environments. Through protograph-based constructions with BCH check nodes, optimized layered min-sum belief propagation decoding, and quasi-cyclic encoding, our designs achieve decoding thresholds 0.45 dB from Shannon limits, with average

iterations under 15 and gate counts of 28k delivering 0.5 dB SNR gains over 5G Polar codes and 0.7 dB over quasi-cyclic LDPC at FER= 10^{-6} for blocklengths $n=256$ (R=0.5, Rician K=12 dB channels).

Simulation results, corroborated by density evolution and EXIT charts, confirm suppressed error floors below 10^{-8} , sub-millisecond latency (420 μ s on CPU, 0.4 μ s FPGA), and energy efficiency at 15 pJ/bit 50% superior to benchmarks, aligning with green 6G sustainability goals by curtailing operational carbon emissions in dense deployments (10^4 femtocells/km²). Comparative evaluations highlight GLDPC's Pareto optimality in the complexity-performance plane, sustaining 95% URLLC compliance amid multi-cell interference (SINR=10 dB).

Implementation insights underscore seamless integration with massive MIMO (64x8 ZF) and edge computing, mitigated challenges like handover via structured storage, paving the way for real-world applications in smart agriculture, healthcare, and cultural heritage preservation. Future directions include AI-augmented neural decoders for adaptive complexity, reconfigurable intelligent surface synergy, and extensions to terahertz bands ensuring equitable, ethical advancement toward intelligent 6G ecosystems.

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