IMPLEMENTATION OF POLAR CODES USING VERILOG HDL

[1]P.JayaPriya, [2]V. M. Kothandathiliban
[1]PG Scholar, Department of ECE, Sri Vidya College of Engineering & Technology, Virudhunagar, Tamil Nadu, India.
[2]Assistant Professor & Head of the Department, Department of ECE, Sri Vidya College of Engineering & Technology, Virudhunagar, Tamil Nadu, India.
[1]jayapriya18032002@gmail.com, [2]kothandathiliban1188@gmail.com

Abstract: Polar codes are error correction codes that are widely used in communication systems. Polar codes exhibits high error correction capability as compared with other error correction codes. This paper proposes a Very Large Scale Integration (VLSI) architecture for the implementation of Polar decoder. Soft-in-soft out decoders, interleavers and deinterleavers is used in the decoder side which employs Maximuma- Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this paper uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. The proposed system has designed by using Verilog HDL and this design was simulated in Xilinx ISE 13.2. 5Gpeakmobile broad band data rates are expected to be around20Gbps. Beyond5G systems are expected to operate at Terabit/s data rates. Today's most advanced polar code implementations currently deliver only around 5Gbps. Therefore, Turbo codes and LDPC codes that played key enablers in 3Gand 4G systems are already unproven for many new 5G applications. Polar code is believed as prominent breakthrough in 5G. It guarantees apical performance for 5G scenarios and hence it is considered as a promising candidate for the5GNewRadio. This work accentuates on the suitability of polar codes for the 5G scenarios.

Key words: Polar Codes, VLSI, VerilogHDL, MAP Algorithm, SISO Decoder, 5G, Interleaver.

Corresponding Author: V. M. Kothandathiliban
Assistant Professor & Head of the Department, Department of ECE, Sri Vidya College of Engineering & Technology, Virudhunagar, Tamil Nadu, India.
E-Mail Id: *kothandathiliban1188@gmail.com*

I. Introduction:

VLSI Design presents state-of-the-art papers in VLSI design, computer-aided design, design analysis, design implementation, simulation and testing. Its scope also includes papers that address technical trends, pressing issues, and educational aspects in VLSI Design. The Journal provides a dynamic high-quality international forum for original papers and tutorials by academic, industrial, and other scholarly contributors in VLSI Design. The development of microelectronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60’s saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60’s when around 100 transistors could be placed on a single chip. It was the time when the cos tf research began to decline and private firms started entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit revolution. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the growth of transistor count to about 1000 per chip called the Large Scale Integration. By mid-eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die.

The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, STMicroelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc. In 1980s, hold-over from outdated taxonomy for integration levels obviously influenced from frequency bands, i.e. HF, VHF, and UHF. Sources disagree on what is measured (gates or transistors) SSI – Small-Scale Integration (0-102) MSI – Medium-Scale Integration (102 -103) LSI – Large-Scale Integration (103 -105) VLSI – Very Large-Scale Integration (105 - 107) ULSI – Ultra Large-Scale Integration (>= 107) VLSI Technology, Inc. was a company which designed and manufactured custom and semi-custom ICs.

The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose, California. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products. The company was founded in 1979 by a trio from Fairchild Semiconductor by way of Synertek - Jack Balletto, DanFloyd ,and Gunnar Wetlesen-and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design) magazine. Alfred J. Stein became the CEO of the company in 1982. Subsequently VLSI built its first fab in San Jose; eventually a second fab was built in San Antonio, Texas. VLSI had its initial public offering in 1983, and was listed on the stock marketas (NASDAQ: VLSI). The company was later acquired by Philips and survives to this day as part of NXP Semiconductors. The first semiconductor chips held two transistors each.

Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now retrospectively as small scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra- large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinction smoot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use. As of early 2008, billion-transistor processors are commercially available. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing new challenges such as increased variation across process corners).

A notable example is NVidia’s 280 series GPU. This GPU is unique in the fact that almost all of its1.4billion transistors are used for logic, in contrast to the Itanium, whose large transistor count is largely due to its 24 MB L3 cache. Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high performance logic blocks like the SRAM (Static Random Access Memory) cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability)[citation needed]. VLSI technology is moving towards radical level miniaturization with introduction of NEMS technology. A lot of problems need to be sorted out before the transition is actually made.

II.LITERATUREREVIEW

Polar codes have gained significant attention in recent years due to their ability to achieve channel capacity with low computational complexity. Since their introduction, numerous research works have focused on improving their performance, decoding efficiency, and hardware implementation.

E. Arıkan [1] introduced the concept of channel polarization and demonstrated that polar codes can achieve the capacity of binary-input discrete memoryless channels. This work laid the theoretical foundation for polar coding and established its importance in modern communication systems. However, the original Successive Cancellation (SC) decoding algorithm suffers from poor performance at short block lengths.

To improve decoding performance, Tal and Vardy [2] proposed the Successive Cancellation List (SCL) decoding algorithm, which maintains multiple decoding paths and significantly enhances error correction capability. Although SCL decoding improves performance close to maximum likelihood decoding, it increases hardware complexity and memory requirements.

Niu and Chen [3] introduced CRC-aided polar codes, where a Cyclic Redundancy Check (CRC) is concatenated with polar codes to improve decoding reliability. This method enhances the performance of SCL decoding and has been widely adopted in practical systems such as 5G.

Further improvements were proposed by Niu et al. [4], who developed rate-compatible punctured polar codes to provide flexibility in coding rates. This approach is particularly useful in adaptive communication systems where varying channel conditions require dynamic rate adjustment.

Balatsoukas-Stimming et al. [5] proposed an LLR-based SCL decoding architecture, which reduces hardware complexity and improves decoding efficiency. Their work demonstrated that using Log-Likelihood Ratios (LLR) instead of probabilities significantly reduces computational requirements, making it suitable for VLSI implementation.

Xin-Yu Shih et al. [6] presented a LEGO-based VLSI architecture for polar encoder using radix-2 processing elements. Their design achieved high throughput and low power consumption, making it suitable for high-speed communication systems.

Rahul Shrestha et al. [7] proposed a high-throughput polar decoder architecture for 5G New Radio applications. Their work focused on optimizing the processing elements to reduce critical path delay and improve overall system performance.

Kavi Priya et al. [8] developed a radix-k based polar encoder architecture, which improves processing speed and scalability for next-generation wireless communication systems.

Despite these advancements, existing systems still face challenges such as:

- High hardware complexity in SCL decoders
- Increased power consumption
- Latency in iterative decoding

Therefore, there is a need for an efficient VLSI architecture that balances performance, complexity, and power consumption. The proposed work addresses these challenges by implementing a MAP-based polar decoder with optimized architecture.

III.PROPOSEDWORK

In a communication system, when data is transferred from the source system to a destination system, errors can be present in the received signal at the source end. So error correction is required to retrieve the original message. Polar codes, which were first introduced in 1993, represent a quantum leap in channel coding techniques and a turning point for modern digital telecommunication. Polar codes is one of existing powerful error correcting codes. Polar codes has inspired the coding community with the possibility of using an iterative decoding technique that relies solely on simple constituent code to achieve close channel capacity. Polar coder architecture comprises of polar encoder and polar decoder. Encoder consists of two Recursive Convolutional Encoders (RSC) and interleaver. In this paper, pseudo-random interleaver is used due to which the interleaved version of the code tends to be long and scrambled, that gives good performance of random codes. In polar code implementation, RSC encoders are employed rather than conventional convolutional encoders since it generates low weight parity codes. MAP algorithm is used for the decoding of polar encoded data in which errors are intentionally added and verified an error free decoded data after decoding.

Polar encoder and decoder together comprises the Polar coder architecture as shown in Figure 1.Two identical Recursive convolutional encoders(RSC) and a pseudorandom interleaver constitutes the polar encoder as shown in Figure 2..LTE employs a 1/3rateparallel concatenated polar code. Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data.

A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The RSC1 and RSC2 encoder outputs along with systematic input comprises the output of polar encoder, that is, a 24-bit output is generated which is illustrated in Figure 2.

This will be transmitted through the channel to the Polar decoder. A standard polar decoder block diagram is shown in Figure3that contains two modules of SISOdecoders together with two pseudorandom interleavers and a pseudorandom deinterleaver.

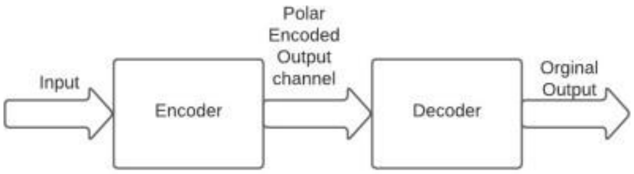


Figure 1. POLAR CODER BLOCK DIAGRAM

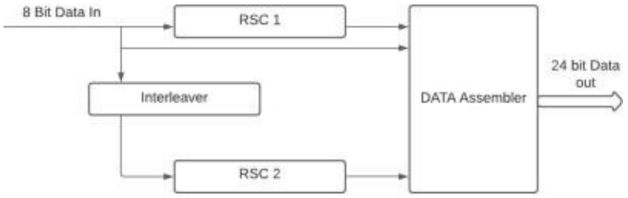


Figure 2. POLAR ENCODER BLOCK DIAGRAM

The usually used method of polar code decoding is carried out using the BCJR algorithm. The fundamental and basic idea behind the polar decoding algorithm is the iteration between the two SISO part decoders which is illustrated in figure 3. It comprises a pair of decoders, those which work simultaneously in order to refine and upgrade the estimate of the original information bits. The first and second SISO decoder, respectively, decodes the convolutional code generated by the first or second CE. A polar-iteration corresponds to one pass of the first component decoder which is followed by a pass of the second component decoder.

The signal which is received at the input of a soft-in- soft-out (SISO) decoder is the real (soft)value of that signal. An estimate of each input bit. The decoder then generates an approximation for each data bit expressing the probability that the transmitted data bit is equal to one. The maximum a- posteriori (MAP) algorithm is used in the polar-decoder under consideration in this paper for the SISO component decoder.

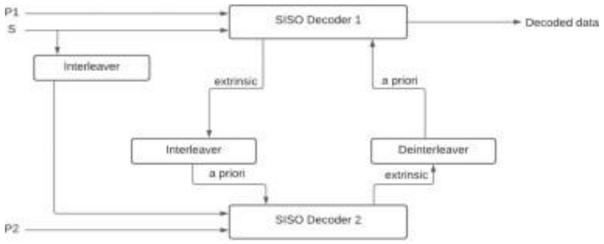


Figure 3. POLAR DECODER BLOCK DIAGRAM

The MAP algorithm never restricts the set of bit estimates to correspond strictly to a valid path through the trellis. Therefore, the results produced by a Viterbi decoder that recognizes the most likely true path through the trellis should differ from those generated by that. AES can be implemented either in software or hardware.

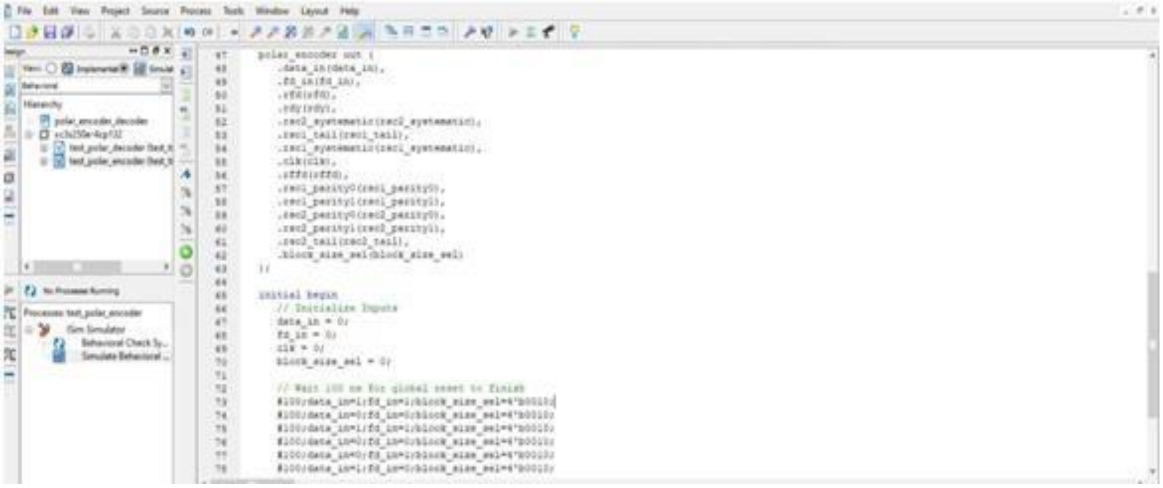
Software implementation requires less resources and cost and its implication also limited, having low seed. Nowadays we require large volume data and high speed requirements made it to implement in hardware. Hardware nothing but we have application specific IC and FPGA. FPGA is reconfigurable device which supports wide range of functionality than ASIC. So we prefer FPGAS to implement AES.

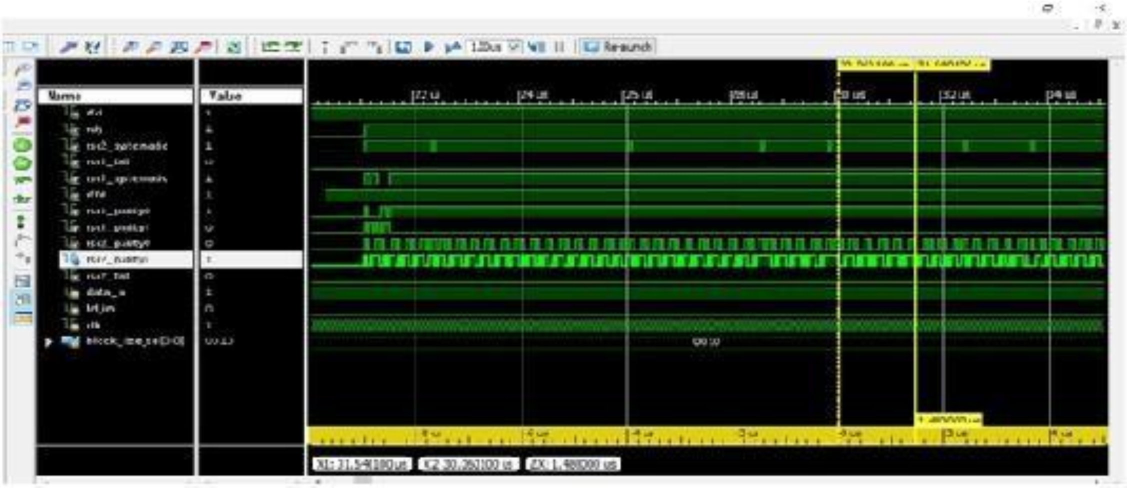
Interleaving is a tool that is used to enhance existing error correcting codes so that they can be used to perform burst error corrections as well. Most error correcting codes (ECCs) are designed to correct random errors, i.e. error caused by additive noise that is independent of each other. Burst errors are the errors that occur in a sequence or as groups. They are caused due to defects in storage media or disruption in communication signals due to external factors like lightning etc. Interleaving modifies the ECC or does some processing on the data after they are encoded by ECCs.

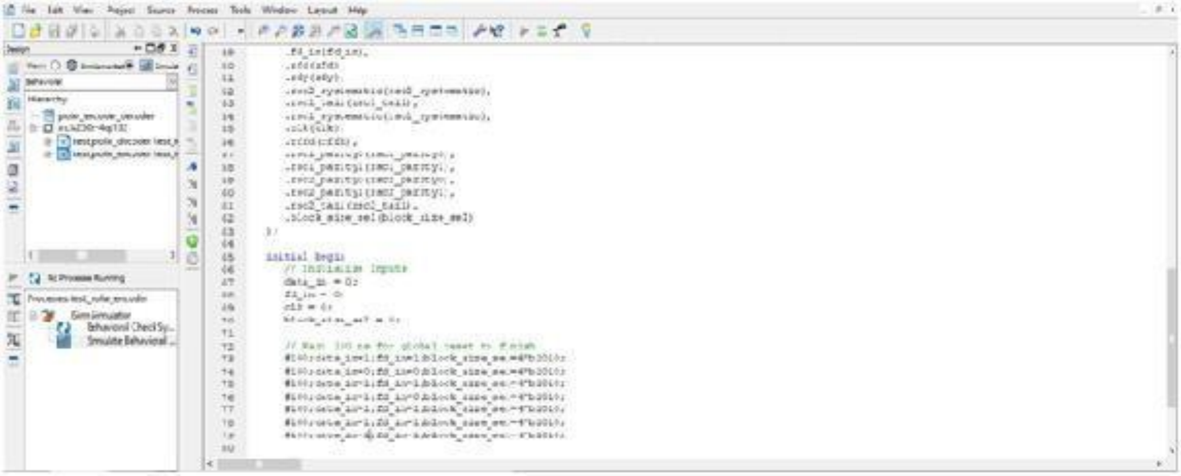
IV.RESULTS AND DISCUSSIONS

For Encoder, Here the data_in1010011 andfd_in1010100 is transmitted for every 100µ seconds and the blocksize is 0010.

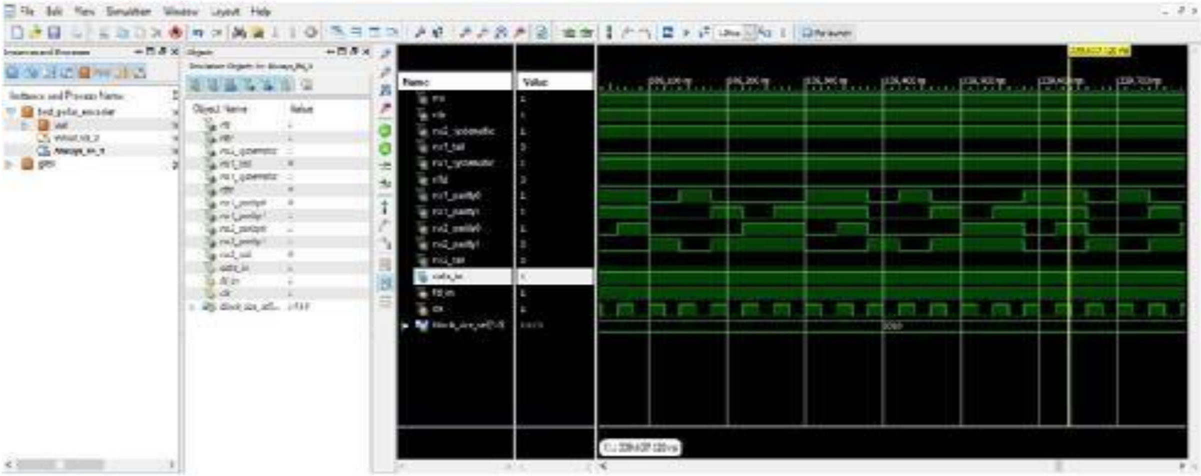
We can observe the block size 0010 and data_in1 and d_in0 is transmitted and the transition occurred at edge of clock as shown in Figure 4.



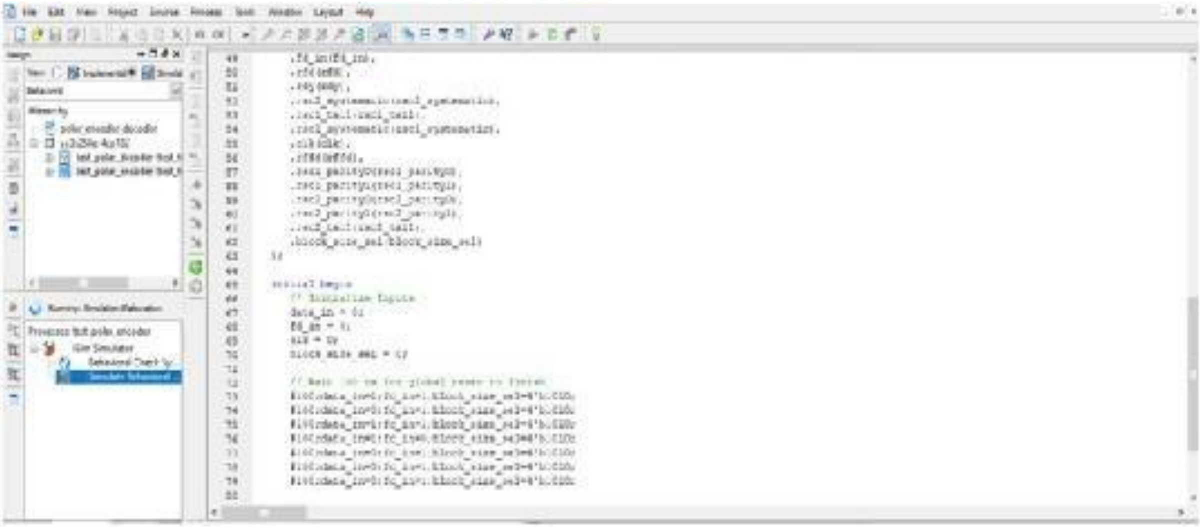




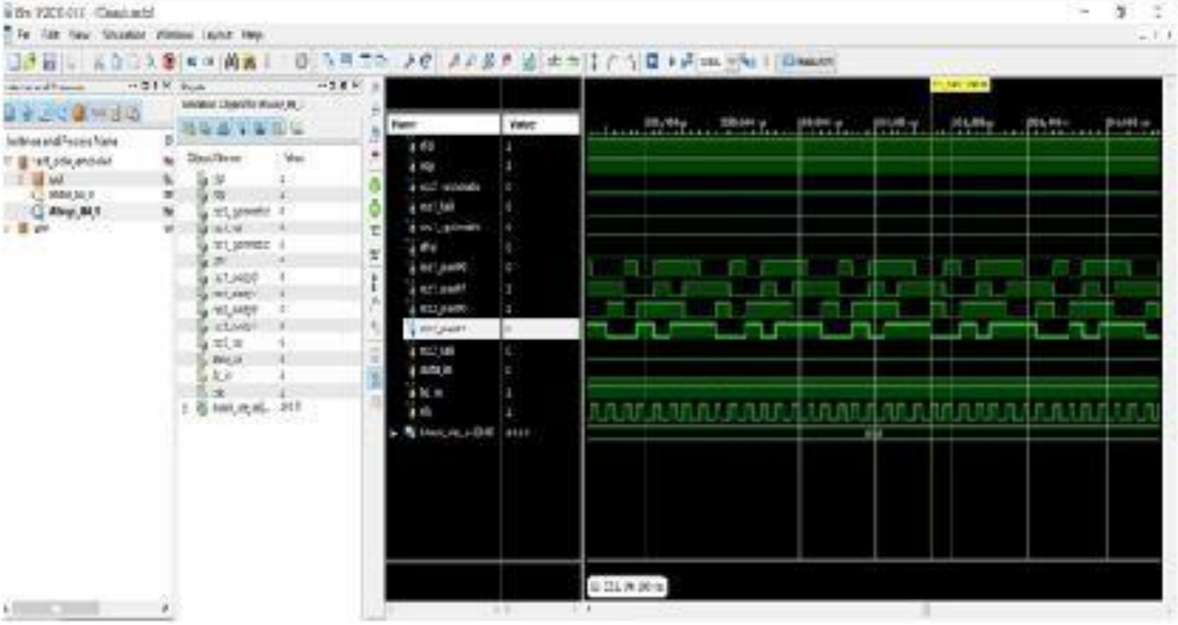
Here the data_in1011111 and fd_in1010111 is transmitted for every 100µ seconds and the block size is 0010.



We can observe the block size 1010 and data_in1 and fd_in1 is transmitted and the transition occurred at edge of clock.

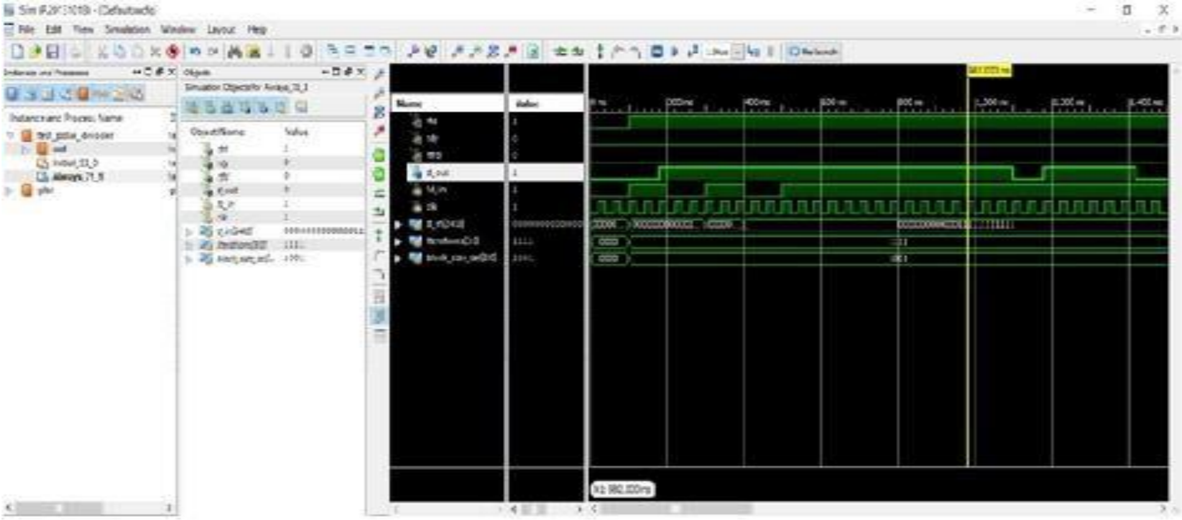


Here the data_in 1011000 and fd_in1110111 is transmitted for every 100µ seconds and the block size is 1010.

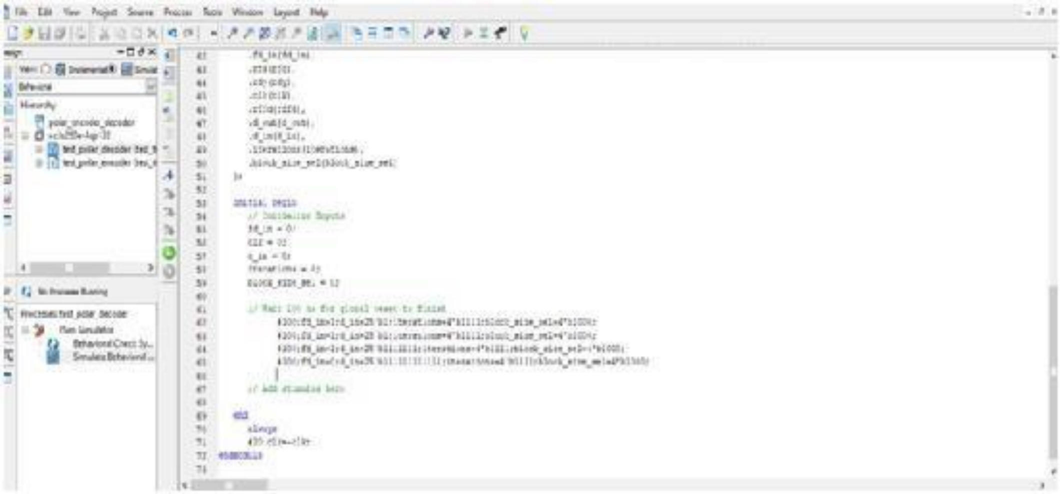


We can observe the block size1010 and data_in0 andfd_in1 is transmitted and the transition occurred at edge of clock.

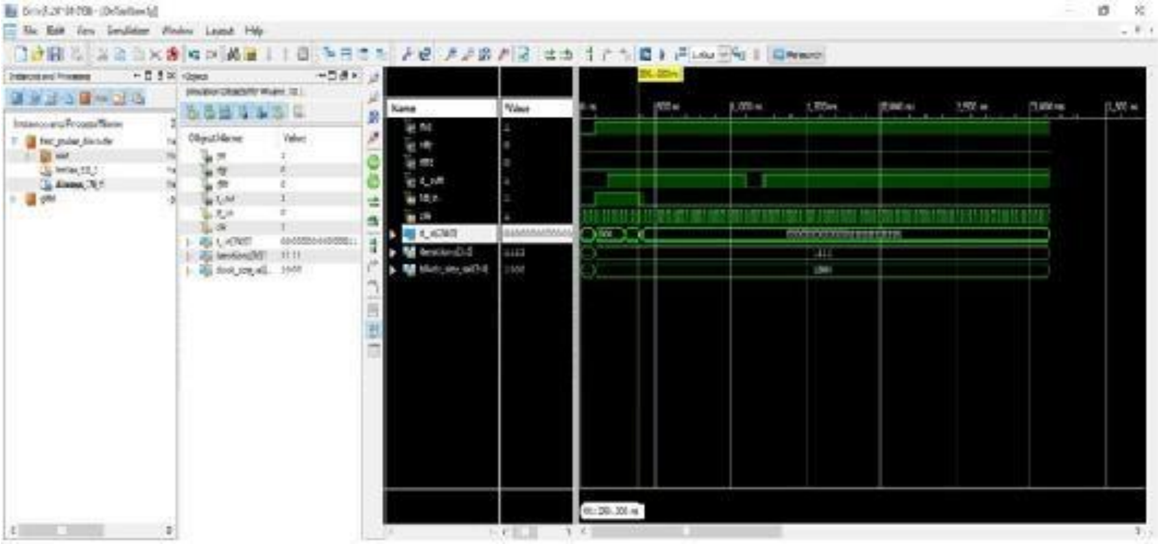
For Decoder, Here the block size is1001 and fd_in 10101 andd_in11111 is transmitted for the given iterations for every 100µ seconds.



We can observe the block size 1001, iterations1111and d_out1 and fd_in1 is transmitted and the transition occurred at edge of clock.

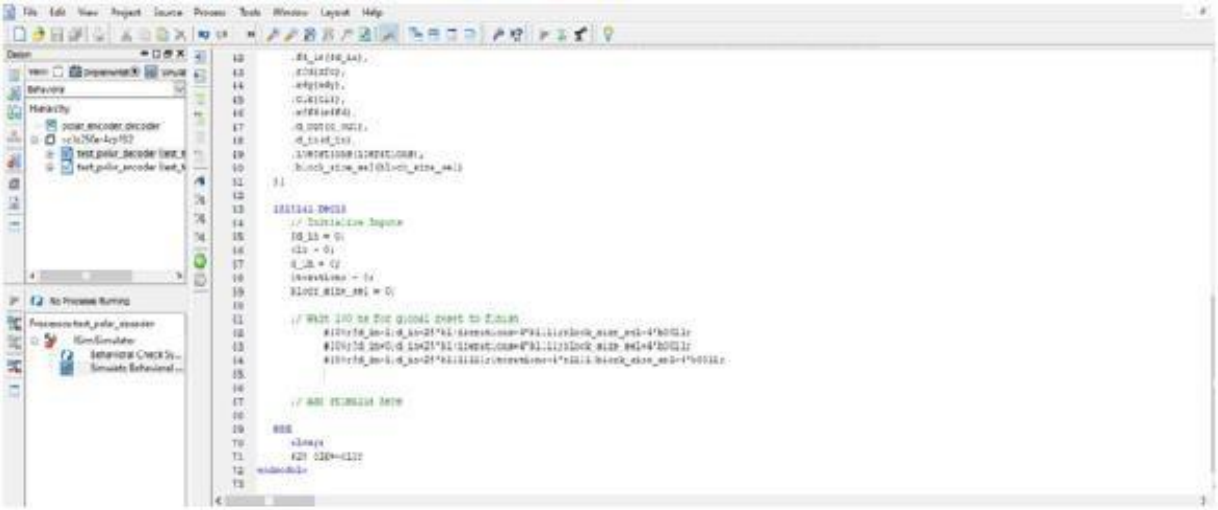


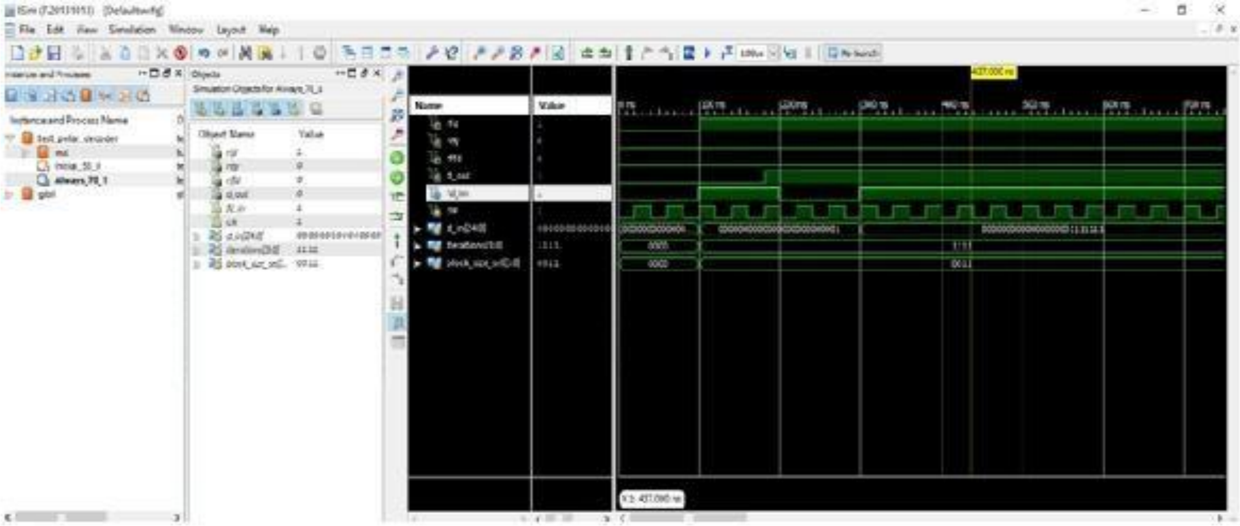
Here the block size is1000 andfd_in1110 and d_in11111 is transmitted for the given iterations for every 100µseconds.



We can observe the block size 1000, iterations 1111 and d_out1 and fd_in1 is transmitted and the transition occurred at edge of clock.

Here the block size is 0011 and fd_in1101 and d_in11111 is transmitted for the given iterations for every 100µ seconds.





We can observe the block size 0011, iterations 1111 and d_out1 and fd_in1 is transmitted and the transition occurred at edge of clock.

V. CONCLUSION

The polar encoder and decoder designs are done using Verilog HDL and simulation has done in Xilinx ISE13.2. TheRTLand Technology schematics have observed in XILINX. Synthesis repost has shown the details of our proposed design. This example highlights one of the polar coding schemes (CRC- Aided Polar) specified by 3GPP for New Radio control channel information (DCI,UCI)and broadcast channel(BCH). It shows the use of components for all stages of the processing (encoding, rate-matching, rate-recovery and decoding) and uses them in a link with QPSK over an AWGN channel. Highlighted performance results for different code rates and message lengths show agreement to published trends, within parametric and simulation assumption variations.

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